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Differences Between MC9S12DG128 and MC3S12RG128

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1 Introduction

This document explains the differences between the MC9S12DG128 and MC3S12RG128 microcontrollers. It is intended for designers who wish to migrate from MC9S12DG128 to MC3S12RG128.

The main difference between these devices is that the MC9S12DG128 has on-chip flash and EEPROM, whereas the MC3S12RG128 is a ROM-only device. Consequently, the MC3S12RG128 has no flash or EEPROM module. Also, the MC3S12RG128 does not have a byte flight module.

The MC3S12RG128 is based on a lighter version of the M9S12D family and includes:

- Two controller area network modules (CAN0, CAN4)
- Two serial peripheral interface modules (SPI0, SPI1)
- Two 10-bit analog-to-digital converter modules (ATD0, ATD1)

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- Two serial communication interface modules (SCI0, SCI1)
- One inter-interconnect connect bus module (IIC0)
- Eight pulse-width modulation channels

The voltage regulator on the MC3S12RG128 operates at 3.3 V and 5 V; therefore, this ROM device can be powered from 3.3 V or 5 V. This is not the case for the flash device, which runs from 5 V only.

The following sections show the differences between the MC9S12DG128 and MC3S12RG128 microcontrollers.

2 Detailed Differences

2.1 Core

The MC3S12RG128 can operate at a higher CPU frequency than the MC9S12DG128.

For the MC3S12RG128:

- Operation up to 33 MHz bus speed (single-chip modes only)
- Operation up to 25 MHz bus speed (expanded modes)

For the MC9S12DG128:

- Operation up to 25 MHz bus speed

2.2 Memory

2.2.1 Flash / ROM

The MC3S12RG128 contains 128 KB of ROM, whereas the MC9S12DG128 features 128 KB of flash. These flash or ROM arrays are located at the same addresses (between 0x3FFF and 0xFFFF) on both devices, with an identical paging mechanism.

On the flash device, certain memory locations are linked to the memory writing and protection management. The content on the ROM devices cannot be updated, therefore flash registers disappear. However, a 32-bit cyclic redundancy check (CRC) and the customer part number (SCxxxxxx) are stored in ROM. Exclude this area from any application CRC calculation because the Freescale CRC will cover application software and cannot be predicted by the customer.

Table 1 summarizes memory management changes between MC3S12RG128 and the MC9S12DG128.

Table 1. Memory Management Changes

Addresses	MC3S12RG128	MC9S12DG128
0xFF00 to 0xFF07	8-byte comparison key (see caution)	8-byte comparison key
0xFF08 to 0xFF0B	32 bits CRC value (NVCRx)	Reserved
0xFF0C to 0xFF0E	Device SC part number (3 bytes – NVSCx) loaded in registers RDSCx after reset	0xFF0C: reserved 0xFF0D: Flash Protection Byte loaded into FPROT after reset 0xFF0E: reserved
0xFF0F	Initial value loaded in register ROPT after reset (NVOPT)	Initial value loaded in the register FSEC after reset

CAUTION

On mask-ROM devices, the backdoor key is also used to protect access to internal product analysis features. No product analysis will be possible on a secured ROM if backdoor key access is disabled or keywords are invalid.

2.2.1.1 Flash/ROM Configuration Registers

The flash configuration registers of the MC9S12DG128 are located between the addresses 0x0100 and 0x010F. On the MC3S12RG128, these registers are replaced with ROM configuration registers and are located on the same locations, excepting those defined in Table 2.

Table 2. Flash Configuration Registers

Address	MC9S12DG128	MC3S12RG128
0x0100	Flash clock divider register (FCLKDIV)	Reserved
0x0101	Flash security register (FSEC)[1]	ROM option registers (ROPT)[2]
0x0102	Reserved – flash test mode (FTSTMOD)	Reserved
0x0103	Flash configuration register (FCNFG)	ROM configuration registers (RCNFG)
0x0104	Flash protection register (FPROT)[1]	Reserved
0x0105	Flash status register (FSTAT)	Reserved
0x0106	Flash command register (FCMD)	Reserved
0x0107–0x010B	Reserved	Reserved
0x010C	Reserved	ROM device SC number register 0 (RDSC0)[2]
0x010D	Reserved	ROM device SC number register 1 (RDSC1)[2]
0x010E	Reserved	ROM device SC number register 2 (RDSC2)[2]
0x010F	Reserved	Reserved

NOTES:
1 These registers are loaded from flash locations.
2 These registers are loaded from ROM locations.

2.3 RAM

MC9S12DG128 and MC3S12RG128 feature 8 KB of RAM. Depending on the value of the INITRM register, these RAM array may have different locations. They are mappable to any 8K boundary.

2.3.1 EEPROM

The MC9S12DG128 features 2 KB EEPROM. Depending on the configuration of the INITEE register, the 2 KB EEPROM array can be mapped to any 2K boundary.

The MC3S12RG128 has no EEPROM. The location between 0x0800 and 0x0FFF is free for the RAM array.

The EEPROM configuration registers are present on the MC9S12DG128 but not on the MC3S12RG128. Memory locations used by these registers on the MC9S12DG128 are marked as reserved on the MC3S12RG128, as illustrated in Table 3.

Table 3. EEPROM Configuration Registers

Address	MC9S12DG128	MC3S12RG128
0x0012	INITEE register	Reserved
0x0110– 0x011B	EEPROM control register	Reserved

2.4 Registers

2.4.1 VREG Configuration Registers

The MC9S12DG128 has a simple voltage regulator (V1), whereas the MC3S12RG128 is equipped with a dual-output voltage regulator. This new version of the regulator has one status and configuration register that the MC9S12DG128 does not have. To maintain compatibility, do not to write at this location in your flash device.

Table 4. Voltage Regulator Configuration Register

Address	MC9S12D64	MC3S12R64
0x0019	Reserved	VREGCTRL

2.4.2 Device ID and MEMSIZE Registers

The PARTIDH and PARTIDL registers represent the part ID of the die in the microcontroller. The different values for MC3S12RG128 and MC9S12DG/DT128 are represented in Table 5.

Table 5. Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC3S12RG128	2M38B	0x0682
MC9S12DT128	1L40K	0x0111
MC9S12DT128	3L40K	0x0113
MC9S12DT128	4L40K	0x0114
MC9S12DT128	5L40K	0x0115

NOTES:
[1] The coding is as follows:
Bit 15–12: major family identifier
Bit 11–8: minor family identifier
Bit 7–4: major mask set revision number including FAB transfers
Bit 3–0: minor, non-full, mask set revision

2.5 Peripherals

Two peripherals are different on the MC9S12DG128 and on the MC3S12RG128.

2.5.1 Voltage Regulator

The MC9S12DG128 has a simple voltage regulator (V1) whereas the MC3S12RG128 is equipped with a dual output voltage regulator. This new version of regulator has one status and configuration register that is not present on the MC9S12DG128. See Section 2.4.1, “VREG Configuration Registers,” for details

2.5.2 ATD Converter

The electrical specifications and the software interface of the ATD converters are the same on the MC3S12RG128 and on the MC9S12DG128; however, if the procedures recommended in the data sheet are not followed, the ATD converters of the flash and of the ROM versions may behave differently. These procedures are detailed in Section 8.5, "Initialization/Application Information,” of Chapter 8, “Analog-to-Digital Converter (ATD10B8CV3),” in the MC9S12RG128 data sheet.

Refer to the erratum MUCts03391 in the errata sheets of the MC3S12RG128 (mask set 2M38B) to confirm that the flash software will also work on the ROM.

3 Errata

Table 6 lists the MC9S12DT128 (3/5L40K mask set) and MC3S12RG128 (xM38B mask set) errata.

Table 6. Errata

Erratum Number	Headline	MC9S12DT128		MC3S12RG128	
		3L40K	5L40K	1M38B	2M38B
MUCts00708	SPTEF flag set erroneously	Yes	Yes	No	No
MUCts00735	ATD flags in ATDSTAT0 do not clear by writing 1, ETORF erroneously set	Yes	Yes	No	No
MUCts00742	SPI in Mode Fault state, but MISO output buffer not disabled.	Yes	Yes	No	No
MUCts00755	BDM STOP mode issue	Yes	Yes	No	No
MUCts00756	MSCAN: Glitch filter exceeds spec limits	Yes	Yes	No	No
MUCts00757	KWU: Glitch filter exceeds spec limits	Yes	Yes	No	No
MUCts00778	Tx messages of same ID block transmission of subsequent lower priority IDs	Yes	Yes	No	No
MUCts00784	Write to ATDCTL5 may not clear SCF, CCF, and ASCIF flags.	Yes	Yes	No	No
MUCts00799	MISO not kept after sixteenth SCK edge.	Yes	Yes	No	No
MUCts00803	FIFO Not Empty Status flag bit problem (3L40K)	Yes	Yes	No	No
MUCts00821	PLL: If osc_clock is 2 to 3 times pll_clock, STOP can cause SCM or reset	Yes	Yes	No	No
MUCts00833	Cumulative EEPROM W/E cycle limit for V & M temp rated products	Yes	No	No	No
MUCts00982	fts128k: STOP instruction while NVM CCIF=1	Yes	Yes	No	No
MUCts00990	eets2k: STOP instruction while NVM CCIF=1.	Yes	Yes	No	No
MUCts01011	ECT: Input pulse shorter than delay counter period recognized as valid	Yes	Yes	No	No
MUCts01029	CCF flags in ATDSTAT1 might fail to set	Yes	Yes	No	No
MUCts01039	Writing ATDCTL5 may not clear CCF flags in ATDSTAT1	Yes	Yes	No	No
MUCts01053	SPIDR can be written without reading SPTEF flag as set.	Yes	Yes	No	No
MUCts01093	MSCAN: Data byte corrupted in receive buffer	Yes	No	No	No
MUCts01103	MSCAN: Time stamp corrupted in receive buffer	Yes	Yes	No	No
MUCts01369	Message erroneously accepted if bus error in bit 6 of EOF (also known as “C and S bug”)	Yes	No	No	No
MUCts01966	Possible manipulation of return address when exiting BDM active mode	Yes	Yes	No	No
MUCts02378	EEPROM program failure during sector-modify	Yes	Yes	No	No
MUCts02415	Missing ECLK edge on first external access after mode switching	Yes	Yes	Yes	Yes
MUCts02960	MSCAN: Potential byte corruption when FIFO full	No	No	Yes	No
MUCts03473	ATD: Abort of an A/D conversion sequence with write to ATDxCTL0/1/2/3 may not work	Yes	Yes	No	No
MUCts03391	ATD: Abort of an A/D conversion sequence with write to ATDxCTL0/1/2/3 may not work	No	No	Yes	Yes

4 Conclusion

The flash and ROM versions can use the same code, therefore you do not need to revalidate the whole application. However, you must take precautions to avoid any conflict. When submitting a ROM code, a Freescale field engineer can advise you and check your code for potential issues.

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